

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15, 19, and 38-44 are in this application. Claim 15 has been amended. Claims 38-44 have been added to alternately and additionally claim the present invention. Claims 1, 5, 6, 10, 11, 17, 18, 20-23, and 33-37 have been cancelled.

The Examiner rejected claims 15 and 19 under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) in view of the Admitted Prior Art (APA). For the reasons set forth below, applicant respectfully traverses this rejection.

Amended claim 15 recites, in part,

an electrostatic discharge (ESD) negative ring;
a plurality of ESD positive lines, the plurality of positive lines not being connected to a steady voltage source; [and]
a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

In rejecting claim 15, the Examiner pointed to "the lines between the high power supply terminals and line R1" shown in FIG. 2 of Gens as constituting the plurality of ESD positive lines. Applicant, however, can find no lines connected between the high power supply terminals VDD₁ and VDD₂ and line R1. As a result, applicant assumes that the Examiner is referring to the two short vertical line segments which have top ends connected to line R1 and bottom ends connected to the cathodes of the diodes (D1) whose anodes, in turn, are connected to high power supply terminals VDD₁ and VDD₂.

These two short vertical line segments, however, can not be read to be the plurality of ESD positive lines because amended claim 15 requires that the plurality of positive lines not be electrically connected together. As shown in FIG. 2 of Gens, the two short vertical line segments are electrically connected together via bus R1.

The Examiner alternately rejected claim 15, arguing that it would have been obvious to connect the ESD switches (130) shown in applicant's FIG. 1 between the positive line and the negative ring in Gens in order to provide more effective unidirectional flow of current during ESD operation. However, even if this were true, Gens, when modified as suggested

by the Examiner, would still show that the two short vertical line segments (read by the Examiner to be the positive lines) are electrically connected together via bus R1.

As a result, claim 15 is patentable over Gens in view of the APA. In addition, since claim 19 depends from claim 15, claim 19 is also patentable over Gens in view of the APA. Further, new claims 38-44 depend either directly or indirectly from claim 15 and are therefore patentable for the same reasons as claim 15.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

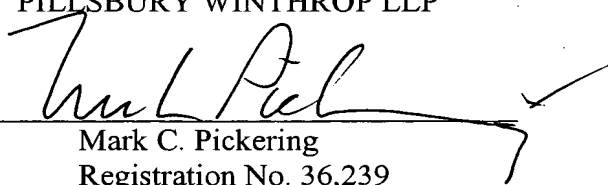
Respectfully submitted,

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APPENDIX

In the Claims

Please cancel claims 1, 5, 6, 10, 11, 17, 18, 20-23, and 33-37.

Please amend claim 15 as follows:

15. (Twice Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:
a plurality of pads;
an electrostatic discharge (ESD) negative ring;
a plurality of ESD positive lines, the plurality of positive lines not being connected to a steady voltage source, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and a negative line;

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

New claims 38-44 have been added.